PATENT

Appl. No. 09/802,291
Amdt. dated April 7, 2004
Reply to Office Action of January 29, 2004

Amendments to the Specification:

Please replace paragraph beginning on page 1, line 6, with the following amended paragraph:

A1

This application is being filed concurrently with related U.S. patent applications: ~~Attorney Docket Number 016747-00991~~ 09/802,017 filed 03/08/01, entitled "VLIW Computer Processing Architecture with On-chip DRAM Usable as Physical Memory or Cache Memory"; ~~Attorney Docket Number 016747-01001~~ 09/802,289 filed 03/08/01, entitled "VLIW Computer Processing Architecture Having a Scalable Number of Register Files"; ~~Attorney Docket Number 016747-01780~~ 09/802,108 filed 03/08/01, entitled "Computer Processing Architecture Having a Scalable Number of Processing Paths and Pipelines"; ~~Attorney Docket Number 016747-01051~~ 09/802,234 now U.S. Patent No. 6,631,439 issued 10/07/03, entitled "VLIW Computer Processing Architecture with On-chip Dynamic RAM"; ~~Attorney Docket Number 016747-01211~~ 09/802,120 filed 03/08/01, entitled "VLIW Computer Processing Architecture Having the Program Counter Stored in a Register File Register"; ~~Attorney Docket Number 016747-01461~~ 09/801,564 filed 03/08/01, entitled "Processing Architecture Having Parallel Arithmetic Capability"; ~~Attorney Docket Number 016747-01471~~ 09/802,196 filed 03/08/01, entitled "Processing Architecture Having an Array Bounds Check Capability"; ~~Attorney Docket Number 016747-01481~~ 09/802,121 filed 03/08/01, entitled "Processing Architecture Having ~~an Array Bounds Check~~ Field Swapping Capability"; and, ~~Attorney Docket Number 016747-01521~~ 09/802,020 filed 03/08/01, entitled "Processing Architecture Having a Matrix-Transpose Capability"; all of which are incorporated herein by reference.

Please replace paragraph beginning on page 2, line 9, with the following amended paragraph:

A2

Instruction sets typically include one or more compare instructions. These instructions ~~compares~~ compare two input registers so that decisions can be made based upon

A2

the result. For example, a branch in software is a compare function followed by checking the result to decide which branch to follow. The output from the compare instruction travels through a dedicated path to a dedicated output register. However, use of a single dedicated register is undesirable in VLIW systems because two separate data paths may want to access the dedicated register at the same time. To accommodate a single dedicated output register, a VLIW system would schedule compare instructions so that none overlapped. Additionally, use of a dedicated path to the output register consumes die area and increases the circuit complexity.

Please replace paragraph beginning on page 9, line 5, with the following amended paragraph:

A3

Referring next to Fig. 4, the machine code for a floating point compare sub-instruction ("FPCMP") 400 is shown. This sub-instruction uses the register addressing form 400 where *Rs1* is the first input operand, *Rs2* is the second input operand and *Rd* is the output operand. The compare sub-instruction 400 is thirty-two bits wide such that a four-way VLIW processor with ~~an~~ a one hundred and twenty-eight bit wide instruction word 52 can accommodate execution of four sub-instructions 400 at a time. The sub-instruction 400 is divided into an address and op code portions 404, 408. Generally, the address portion 404 contains the information needed to load and store the operators, and the op code portion 408 indicates which function to perform upon the operators.

Please replace paragraph beginning on page 13, line 3, with the following amended paragraph:

A4

After the input operands are loaded, processing may begin. In step 628, the compare operation is performed in the ALU 512. As is well known in the art, a compare is implemented by subtracting the operands and analyzing the result. From this analysis, ~~an~~ a value is formulated which indicates the result. The above Table II provides the integer values used in this embodiment to indicate the various results.